Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original): A method of fabricating a contact pad of a semiconductor device, the method comprising:

(a) forming a gate structure including a gate upper dielectric layer on a semiconductor substrate;

(b) forming a stopping layer over the semiconductor substrate;

(c) forming an interdielectric layer over the stopping layer;

(d) planarizing the interdielectric layer to expose at least the gate upper dielectric layer using a material which exhibits a high-polishing selectivity with respect to the interdielectric layer;

(e) etching the interdielectric layer in a region in which a contact pad will be formed on the semiconductor substrate;

(f) depositing a conductive material for the contact pad on the semiconductor substrate; and

(g) planarizing using a material which exhibits a high-polishing selectivity of the gate upper dielectric layer with respect to the conductive material.

2. (Currently amended): The method of claim 1, wherein the gate upper dielectric layer is one selected from the group consisting essentially of a silicon nitride layer (SiN) and ~~a~~ an aluminum oxide layer (Al_2O_3).

3. (Original): The method of claim 1, wherein the thickness of the gate upper dielectric layer is in the range of approximately 1500 Å and 2500 Å.

4. (Currently amended): The method of claim 1, wherein the stopping layer is a silicon nitride layer (SiN).

5. (Original): The method of claim 1, wherein the thickness of the stopping layer is in the range of approximately 50 Å and 150 Å.

6. (Currently amended): The method of claim 1, wherein the ~~inerdielectric~~ interdielectric layer is dielectric layer selected from the group consisting of a polymer, a ~~HDP~~ high density plasma oxide layer, a ~~PE-TEOS~~ plasma enhanced tetra ethyl ortho silicate glass layer, a ~~USG~~ undoped silicate glass layer, a ~~BPSG~~ boron phosphorous silicate glass layer, a ~~PSG~~ phosphorous silicate glass layer, a ~~FOX~~ flowable oxide layer, and a photoresist layer.

7. (Original): The method of claim 1, wherein a process for planarizing the interdielectric layer is further performed after the depositing of the interdielectric layer.

8. (Currently amended): The method of claim 1, wherein planarizing of (d) is performed using a process chosen from the group consisting essentially of ~~CMP~~ chemical-mechanical polishing and dry etching.

9. (Original): The method of claim 8, wherein the CMP is performed using a slurry which exhibits a polishing selectivity of the gate upper dielectric layer with respect to the interdielectric layer in the range of approximately 1:5 to approximately 1:50.

10. (Currently amended) The method of claim 9, wherein the slurry includes abrasive particles ~~particle~~ selected from the group consisting essentially of alumina, silica, ceria, and manganese oxide (Mn_2O_3).

11. (Original): The method of claim 1, wherein an etch buffering layer is formed on the entire surface of the planarized semiconductor substrate is further performed after (d).

12. (Original): The method of claim 11, wherein an anti-reflective layer is formed on the semiconductor substrate on which the etch buffering layer is formed.

13. (Original): The method of claim 11, wherein the etch buffering layer is formed of the same material as the conductive material.

14. (Original): The method of claim 11, wherein the thickness of the etch buffering layer is in the range of approximately 500 Å and 1500 Å.

15. (Original): The method of claim 12, wherein the anti-reflective layer includes amorphous carbon layer.

16. (Original): The method of claim 1, wherein an exposed portion of the stopping layer is etched after (e).

17 (Currently amended) The method of claim 1, wherein the conductive material for the contact pad is one chosen from the group consisting of polysilicon, ~~titanum~~ titanium (Ti), nitride ~~titanum~~ titanium (TiN), and tungsten (W).

18. (Currently amended): The method of claim 1, wherein planarizing of (g) is performed from a process chosen from the group consisting essentially of dry etching and CMP.

19. (Original): The method of claim 18, wherein the CMP process is performed using a slurry which exhibits a polishing selectivity of the gate upper dielectric layer with respect to the conductive material in the range of approximately 1:5 to approximately 1:50.

20. (Original): The method of claim 19, wherein the slurry includes abrasive particles selected from the group consisting essentially of alumina, silica, ceria, and Mn_2O_3.